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Published in:
Proceedings of 10th IEEE International Conference on Terahertz Electronics

Link to article, DOI:
10.1109/THZ.2002.1037603

Publication date:
2002

Document Version
Publisher's PDF, also known as Version of record

Limitations in THz power generation with Schottky diode varactor frequency multipliers

Viktor Krozer, Member, IEEE, Gabriel Loata, Jesús Grajal de la Fuente and Pablo Sanz

***Abstract*— We discuss the limitations in power generation with Schottky diode and HBV diode frequency multipliers. It is shown that at lower frequencies the experimental results achieved so far approach the theoretical limit of operation for the employed devices. However, at increasing frequencies the power drops with f^3 instead of the f^2 predicted by theory. In this contribution we provide an overview of state-of-the-art results. A comparison with theoretically achievable multiplier performance reveals that the devices employed at higher frequencies are operating inefficiently and the design and fabrication capabilities have not reached the maturity encountered at lower THz frequencies.**

***Index Terms*—Frequency conversion, converters, Schottky diodes, submillimeter wave circuits, submillimeter wave devices.**

I. Introduction

Impressive results with regards to the output power from varactor multipliers have been demonstrated by RPG and others around 1 THz. The difficulty to repeat these results at frequencies above 2.5 THz is due to the fact that the doping concentrations for the Schottky varactor devices employed in these multipliers ought to be well above $1 \cdot 10^{17}/cm^3$. At these doping levels the C_{max}/C_{min} ratio is lowered and the efficiency rapidly deteriorates. Another important factor is the high maturity required for fabrication and design of multiplier circuits.

It is therefore important to understand the limiting mechanisms in varactor based multipliers at THz frequencies and develop design tools, which would enable the optimisation of the varactor device and the multiplier circuit.

In this contribution we present an overview of the achieved experimental and simulated results and show simulations of frequency multipliers up to 2.5 THz. The scope of the paper is to present the theoretical limit for multiplier performance with the existing devices and to demonstrate that advanced simulation and design tools are capable of reproducing the experimental results up to 2.5 THz operating frequencies. Both these simulations are intended for device optimisation and for improved multiplier circuit performance. Details on the advanced simulation tool will be provided below.

II. Review of State-of-the-Art

Most results covering frequency multiplication with Schottky diodes (SD) and heterostructure barrier varactors (HBV) have been experimentally achieved in the frequency below 800 GHz. Some new results exist up to frequencies of 1.5 THz and 2.7 THz. At these frequencies the power is of the order of several μW. The results are shown in Figure 1 and Figure 2 for output power and efficiency versus frequency, respectively.

A remarkable advancement can be observed from the introduction of planar Schottky diodes. Most planar SD outperform the whisker-contacted devices both in output power and efficiency. This is especially true for higher frequencies. This could be partly due to better embedding of the device into waveguide mounts or into quasi-optical structures.

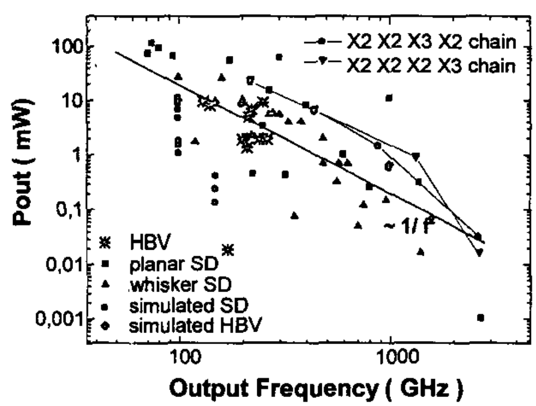

Figure 1: Output power versus frequency for planar, whisker contacted Schottky diodes, HBV devices, and simulated values for Schottky diodes.

Figure 1 and figure 2 show that at lower frequencies below 800 GHz the decrease in output power is determined by the

Manuscript received August 30, 2001. This work was supported in part by the European Space Agency, under contract number 15217/01/NL/FM and 15293/01/NL/FM.

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well-known RC constant of the devices. It drops therefore with the square of the frequency. At higher operating frequencies the experimentally obtained output powers and efficiencies decrease much faster and follow a $1/f^3$ slope. It indicates that either the devices are not utilised optimally or an additional mechanism limits the achievable output power and efficiency.

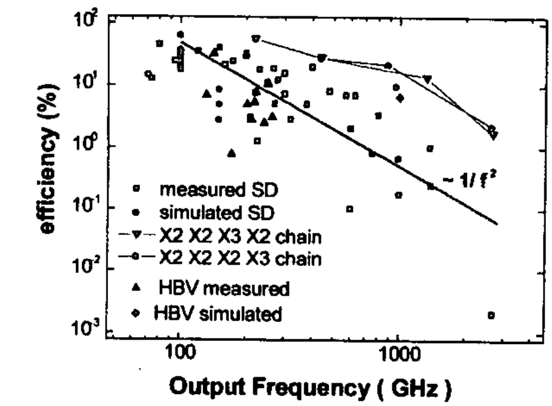

Figure 2: Experimental and simulated conversion efficiency versus frequency for Schottky diodes and HBV devices, and simulated values for Schottky diodes.

This trend can be clearly observed in figure 3, where the zero-bias capacitance and the product of the zero-bias capacitance with the series resistance (inverse of the transit frequency- RC product) has been plotted versus the output frequency. The junction capacitance decreases with the increasing frequency and levels off at frequencies beyond 600 GHz. The RC product follows this change in capacitance and is relatively flat at higher frequencies with a value of 40 fs above 1THz.

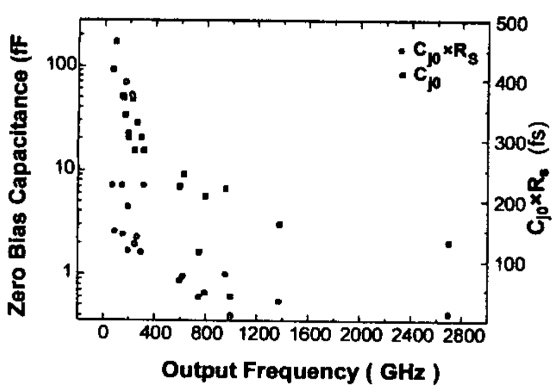

Figure 3: Zero bias capacitance and the inverse of the transit frequency versus frequency for Schottky diode multipliers

At lower frequencies the voltage dependence of the junction capacitance, which is used to achieve frequency multiplication, is limited by the breakdown voltage of the device. At high frequencies the design procedure differs from that at low frequencies because the breakdown voltage is no longer the limiting factor. Hence, maximum output power and conversion efficiency is achieved when current density is smaller than the saturation current. This determines the optimum doping.

It can be assumed that the losses in the waveguide and planar structures are not responsible for this additional decrease in output power at increased frequencies, because these would show up gradually over the frequency.

From our simulations of the theoretical limit of multiplier performance we can confirm this assumption and conclude that the semiconductor devices are responsible for the larger slope in the output power versus frequency. Therefore, it is interesting to identify the possible effects giving rise to this behaviour.

III. THEORETICAL LIMIT FOR MULTIPLIER PERFORMANCE

Individual and cascaded multipliers have been simulated from 100 GHz up to 2.6 THz using Agilent ADS2000 simulator and the built in Schottky diode model. This device model does not account for barrier-lowering, avalanche breakdown, tunnelling, or velocity saturation. It can therefore be used to set a theoretical limit to multiplier performance using a varactor device. The results from these simulations are provided in Figure 1and Figure 2 and details are shown in Figure 4.

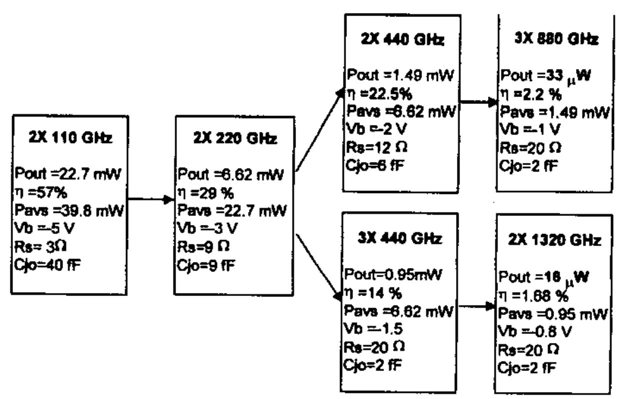

Figure 4: Simulated performance of a multiplier chain up to 2.7 THz.

It can be depicted from Figure 1 and Figure 2 that a major drop in efficiency and power is due to an inefficient utilization of the diode devices. The results presented in the figures are based on the simulation of a multiplier chain, starting with a frequency of 110 GHz fundamental Gunn operating frequency. Two approaches have been investigated

The parameters for devices employed in the simulations are provided in Table 1. The operating conditions can be depicted from Figure 4 and Table 1. Simply scaling the capacitance from previous lower frequency triplers we concluded that a zero-bias capacitance of 2-3 fF is an appropriate starting point for 3×880 GHz. All scaled devices are indicated as SDD in Table 1.

Table 1

	Rs (Ω)	Cjo (fF)	Pout (mW)	η (%)	Z[nfo] (Ω)
2x110 GHz					
UVA 6T2	3	40	22.7 @ 39.8 mW	61.6@ 19.95 mW	10.4+j*99.8 22.3+j*47.1
UVA 5T1	6	20	13.2 @ 25.1 mW	60.7@ 15.84 mW	23.6+j*76.4 46.7+j*77.9
2x220 GHz					
TUD SLV 0910	9	9	5.4@ 12.5 mW	47.5@ 10 mW	36.9+j*162.6 61.3+j*62.2
UVA 5T1	6	20	11.7 @ 31.6 mW	37.9 @ 25.11 mW	12.8+j*77.1 23.6+j*33.7
Approach A: ×2×3					
2x440 GHz					
UVA 2T14	8	5	3.87 @ 10 mW	43.64 @ 7.94 mW	25.7+j*125.6 48.1+j*47.1
UVA 2T2	12	6	3.65 @ 12.5 mW	3.65 @ 12.5 mW	23.8+j*106.8 42.2+j*43.2
3x880 GHz					
SDD 1	15	3	0.99 @ 25.11 mW	4.03 @ 19.95mW	5.27+j*97.7 j*55.04 30.1+j*25.17
SDD 2	20	2	0.78 @ 15.84 mW	5.65 @ 10 mW	9.45+j*148.1 j*85.35 46.32+j*35.0
Approach B: ×3×2					
3x440 GHz					
SDD 3	18	4	1.37 @ 19.95 mW	7.8 @ 12.58 mW	9.6+j*157.8 j*86 44.6+j*38.04
SDD 4	20	2	0.83 @ 5.01 mW	21.3 @ 2.5 mW	28.4+j*323.8 j*180.8 91.9+j*50.4
SDD 5	10	2	0.97@ 2.5 mW	42 @ 1.99 mW	28.7+j 323,7 j 179.2 81.5+j*45.7
2x1320 GHz					
SDD 6	25	1.5	1.14 @ 10 mW	11.9 @ 7.94 mW	50.1+j*90.6 54.7+j*35.2
SDD 7	20	2	1.16 @ 10 mW	11.6 @ 10 mW	34.6+j*70.93 41.3+j*28.97

Table 1: Summary of device parameters employed in simulations. Two distinct approaches are indicated above 440 GHz.

IV. RESULTS FROM PHYSICS BASED SIMULATIONS

The investigation of the electrical characteristics of submillimeter-wave frequency multipliers based on Schottky diodes is performed with a simulation tool which couples the harmonic-balance method and a physics-based drift-diffusion numerical device simulator [2]. Our simulator incorporates accurate boundary and interface conditions for self-consistent treatment of tunnelling transport, image-force effects, and non-constant recombination velocity. Impact-ionisation is also included in the simulator.

This simulator allows us to concurrently design the multipliers taking into account both the device structure (doping and length of the epilayer, and area of the device) and the embedding circuit (bias, available power and loads at different harmonics).

One important conclusion of the analysis of the multiplier chain with this simulator, Table 2, is that the predicted efficiencies are much lower than the ones presented in Table 1. The main reason is that this physics-based simulator accounts for limiting mechanisms such as avalanche breakdown, velocity saturation, and increase in the series resistance with the input power [2].

Table 2

	Pout (mW)	η (%)
2x110 GHz		
UVA 6T2	7.1 @ 40 mW	28 @ 13 mW
2x220 GHz		
TUD SLV 0910	4.0 @ 40 mW	14 @ 6.3 mW
Approach A: ×2×3		
2x440 GHz		
UVA 2T14	Figure 5	
3x880 GHz		
UVA 2T14	Figure 6	
Approach B: ×3×2		
3x440 GHz		
UVA 2T14		1.6 @ 2.5 mW
UVA 2T14[b]		2.5 @ 1 mW
2x1320 GHz		
UVA 2T14		5 @ 1 mW

Table 2: Summary of the multipliers analysed with the physical numerical simulator.

On the other hand, it is possible to identify several shortcomings in the design of a multiplier chain that degrade its performance in terms of available output power.

- The aim in the different stages of the multiplier chain is to maximise the output power at the desired harmonic. If the available input power is high enough, we can maximise the output power at the expenses of the conversion efficiency. However, maximisation of the output power for a fixed input power implies maximisation of the efficiency. An adequate selection of the anode area is sufficient to solve this problem. Figure 5 shows the conversion efficiency for a 2x440GHz doubler based on the varactor *UVA 2T14* [6]. It is clear that there is an optimum area for a fixed available input power. The conversion efficiency obtained in the multiplier chain of figure 4 is much lower than the maximum conversion efficiency predicted in table I. If the area of the varactors of the last two stages had been properly scaled down, the total efficiency of the chain would have increased.

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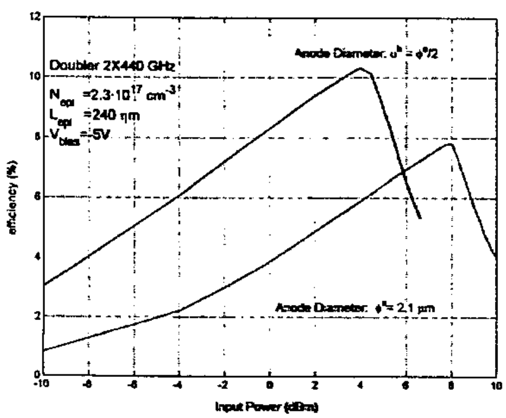
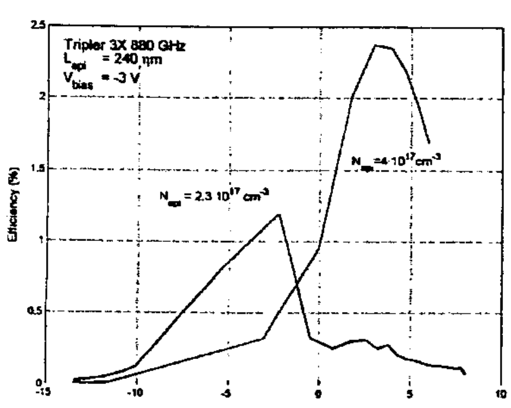


Figure 5: Conversion efficiency for two doublers 2x440 GHz. The varactor is UVA 2T14 and ϕ^a=2.1μm is the original anode diameter [6].

- The appropriate selection of the doping in the epitaxial layer can alleviate the limitations in the generation of power at harmonics due to velocity saturation. Figure 6 shows the improvement in the conversion efficiency for a tripler 3x880GHz when the doping level in the epitaxial layer changes from $N_{epi}=2.3\cdot10^{17}cm^{-3}$ to



$N_{epi}=4\cdot10^{17}cm^{-3}$.

Figure 6: Impact of epilayer doping on the conversion efficiency. The increase in the epitaxial doping reduces the impact of the velocity saturation.

V. Conclusion

The limitations in power generation with Schottky diode frequency multipliers have been discussed and state-of-the-art published results have been presented. It is shown that at lower frequencies the experimental results achieved so far approach the theoretical limit for the employed devices. However, at increasing frequencies the power drops with $1/f^3$ instead of the $1/f^2$ predicted by theory. This discrepancy is attributed to the inefficient use of the available devices, which indicates that more output power can be expected from frequency multipliers at high operating frequencies.

Simulated results for the theoretical limit in output power and efficiency are presented along with more detailed simulations using advanced physical models. The output power from a multiplier chain has been simulated to be 33μW at 2640 GHz with a cascaded overall efficiency of $8.1\ 10^{-4}$. These efficiencies although low still outperform the best photonic mixer efficiencies published so far, which is a potential alternative to frequency multipliers.

Acknowledgment

The authors would like to acknowledge the support from the European Space Agency ESA/ESTEC for partial financial support of this work under contracts: 15217/01/NL/FM and 15293/01/NL/FM.

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